REMARKS

Summary of the Office Action

Claims 1 and 2 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Ohzeki et al.* (U.S. Patent 4,625,241). Claims 3 and 4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ohzeki et al.* in view of *Sakuragi et al.* (US 2002/0109620).

Summary of the Response to the Office Action

Applicant has added new claims 5-7. Accordingly, claims 1-7 are pending for further consideration.

All Claims Define Allowable Subject Matter

Claims 1 and 2 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Ohzeki et al.* (U.S. Patent 4,625,241) and claims 3 and 4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ohzeki et al.* in view of *Sakuragi et al.* (US 2002/0109620). Applicant respectfully traverses the rejection for at least the following reasons.

Independent claim 1, recites, in part, "a counter circuit to which the digitized input signal, a counter clock signal and a trigger signal are provided so as to set a count number based on the digitized input signal and start counting the counter clock signal in response to the trigger signal," (emphasis added). The Office Action suggests that the 3 bit counter 57 in FIG. 6 of *Ohzeki et al.* is the "counter circuit" as claimed in independent claim 1. Applicant respectfully disagrees. Col. 6, lines 33-38 of *Ohzeki et al.* discloses that the "3 bit counter 57" is a three-bit binary counter where its frequency is divided into 8. In *Ohzeki et al.*, each divided bit is output in parallel to "select 56" while the MSB output is to the clock input of "first counter 42" and that

of "latch circuit 55." In this regard, the clock counter itself merely outputs the incoming CK signals to "select 56," "first counter 42," and "latch circuit 55" by repeating the same although the signal is divided. Therefore, *Ohzeki et al.* is completely silent as to a signal representing "count number," as required by claim 1. Accordingly, Applicant respectfully asserts that *Ohzeki et al.* fails to disclose a counter circuit to which the digitized input signal, a counter clock signal and a trigger signal are provided so as to set a count number based on the digitized input signal and start counting the counter clock signal in response to the trigger signal, as required by independent claim 1.

For at least the above reasons, Applicant respectfully asserts that claim 1 is not anticipated by *Ohzeki et al.* As pointed out in MPEP § 2131, "[to] anticipate a claim, the reference must teach every element of the claim." Furthermore, Applicant respectfully asserts that *Sakuragi et al.* does not remedy the deficiency of *Ohzeki et al.* Thus, Applicant respectfully asserts that the rejection under 35 U.S.C. § 102(b) should be withdrawn because *Ohzeki et al.* fails to teach or suggest each feature of claim 1. In addition, Applicant respectfully asserts that dependent claims 2-4 are allowable for the same reasons set forth above.

New Claims 5-7

Applicant has added new claims 5-7 to further define the invention. Applicant respectfully submits that new claims 5-7 are allowable at least because of the combination of features recited therein.

Conclusion

In view of the foregoing, Applicant respectfully requests reconsideration and the timely allowance of all pending claims. Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicant's undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310.

Respectfully submitted,

MORGAN, LEWIS & BOCKIUS LLP

By: _____
Robert J. Goodell
Reg. No. 41,040

Dated: July 18, 2007

MORGAN, LEWIS & BOCKIUS LLP
1111 Pennsylvania Avenue, N.W.
Washington, D.C. 20004
(202) 739-3000